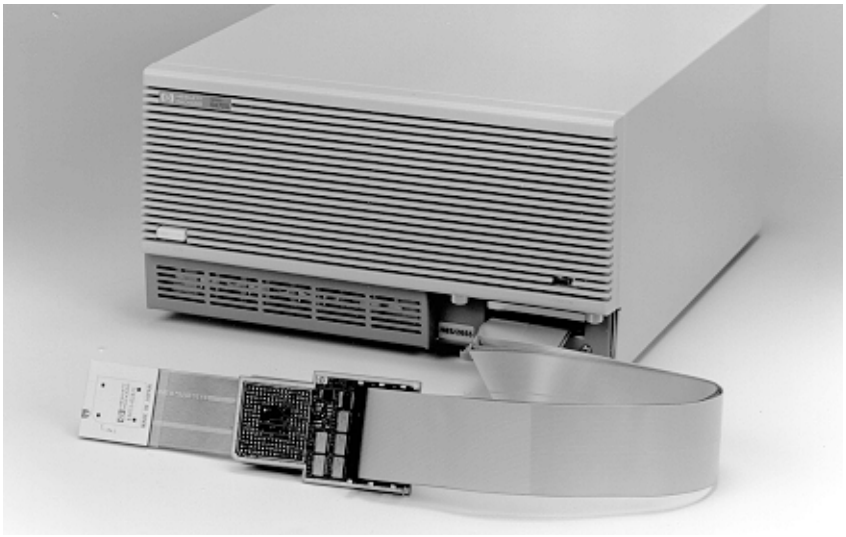
HP E3471A Emulator for Hitachi H8S/2000 Series Microprocessors

Product Overview

Design, debug, and integrate real-time embedded systems

The HP E3471A emulator supports Hitachi H8S/2241, 2242, 2245, 2246, 2653 and 2655 microprocessors to clock speeds of 25 MHz at 5 volts and 13 MHz at 3 volts with no adapter. The emulator provides the capabilities needed to develop H8S/2000 Series embedded systems including; real-time measurements, interpreted displays of on-chip registers, emulation memory, a deep-trace analyzer, and hardware breakpoints.

For both PC and workstation the C debugger user interface is provided, offering a similar look and feel as Microsoft Windows 95 and X/Motif. The debugger combines the ease of use of a full graphical user interface with the HP 64700's transparent, real-time emulation. It provides powerful measurement capabilities ranging from real-time nonintrusive analysis to high-level C source code debugging. This combination allows you to debug embedded C programs at the source level, while your target runs at full speed.



HP E3471A Features

- 25 MHz*, at 5 volts and 13 MHz* at 3 volts
- Zero-wait state in target and emulation memory
- Support for H8S/2241, 2242, 2245, 2246, 2653 and 2655 processors
- Configuration menu for easy emulator setup
- Display and modify functions for internal I/O registers
- Background monitor
- Eight real-time hardware breakpoints
- Unlimited software execution breakpoints
- Support for fast file download
- Connection to the target system
  - Soldered socket adapter for 100, 120 or 128 pin QFP packages
  - Soldered socket adapter can be used by emulator probe or H8S microprocessor
  - A 6 inch flexible probe cable provides a pliable connection between the socket on the target system and the adapter cable
  - A two foot adapter cable connects the HP 64700 system to the probe cable

*Contact your HP 64000 field engineer for the latest configuration information and supported processor speeds.

Modular HP 64700 Series system

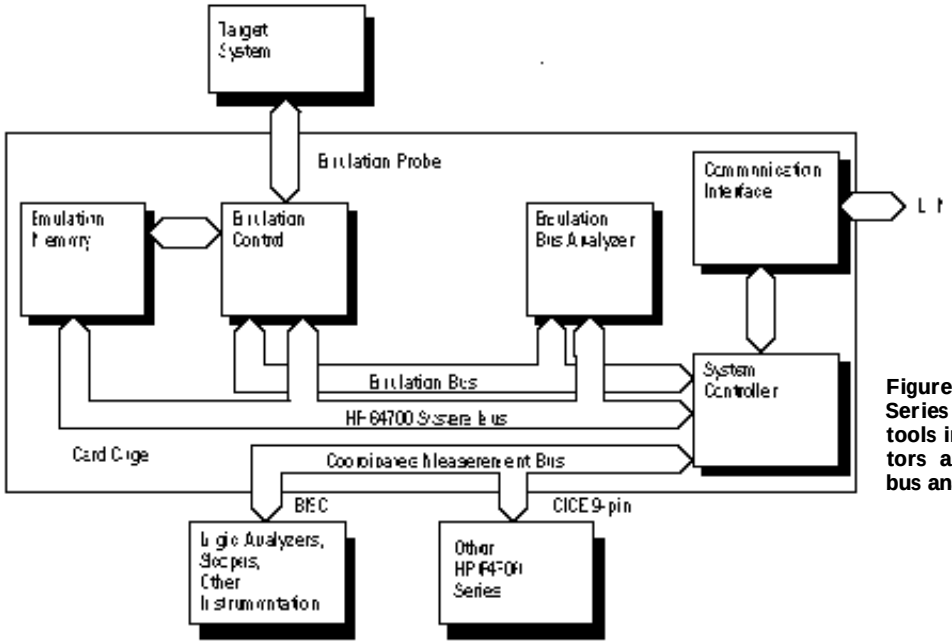


Figure 1. HP 64700 Series development tools include emulators and emulation bus analyzers.

Emulation Bus analyzer

- 80 channel available with trace buffer depths of 1 K, 8 K, 64 K, or 256 K
- Postprocessed software-based dequed trace with symbols and source lines
- Eight hardware breakpoints, each consisting of address, status and data comparators
- Event sequencing up to eight levels deep
- Time tags with 20 nsec resolution (HP 64794X) and state counting
- Prestore capability

Emulation Memory

- Dual-ported emulation memory allows modification of memory without interrupting the processor
- Memory configurations of 256K, 1M and 4M
- Memory mapping in 1K blocks

Software Support

- The C debugger user interface is hosted on a PC or HP 9000 Series 700 workstation*
- The Hitachi assembler and compiler are supported on a PC or HP 9000 Series 700 workstation**

* For support on Sun SPARC workstations contact you local HP sales representative

**For support of IAR SYSTEMS AB assembler and compiler contact your local HP sales representative.

HP 64700B Card Cage

- A modular chassis for emulation tools and analysis tools
- The modular design is easily reconfigured to support 8, 16 and 32 bit microprocessors
- Built-in LAN for maximum system throughput for growing system design needs
- Flash EPROMs for easy and fast firmware updates
- Space for future measurement needs

Networking

In many embedded design environments, it is not possible for every member of a design team to have an emulator. The HP 64700 Series LAN connectivity provides remote access from a networked host. Now you can share a central emulator and target from a PC or workstation. Rapid file transfers—at rates of up to 6 Mbytes per minute—can increase your productivity. The HP 64700B LAN connects to all popular Ethernet 803.2 networks through a 10Base2 (BNC ThinLAN) connector or a 15 pin AUI (attachment unit interface). The system supports TCP/IP protocols, LAN gateways and ARPA/Berkley standards.

Emulation Bus Analysis

Emulation bus analysis provides real-time, nonintrusive operation along with extensive triggering, tracing, and qualification features. Analysis features include selective tracing, time-tagging, pre-store and a choice of 1K, 8K, 64K or 256K trace depths. These comprehensive resources combine to help you solve both simple and complex problems.

With dual-bus architecture you can setup and view traces without breaking processor execution. Selective tracing of microprocessor code flow without interrupting execution is a major strength of the HP 64700 Series emulators and analyzers.

You can combine up to eight hardware breakpoints, each consisting of address, data and status comparators. The HP 64700 Series permits you to specify sequential trace specifications constructs, i.e. “find A, followed by B...” up to eight levels deep. The analyzer will trigger on and store all subsequent executions, or store only specified execution information.

Precise time-tagging of events helps you identify discrepancies in code execution. The analyzer logs each event with its execution time. Bus cycle, instruction, and module duration can be measured at full processor speeds.

Prestore helps pinpoint possible problem areas in the code by determining which of several functions is accessing a variable and is responsible for corrupting it.

Real-Time Emulation

The HP E3471A includes the microprocessor, emulation monitor, run control circuits and up to 4M of dual-port emulation memory. The background monitor uses no target address space.

HP’s high-speed emulation memory requires zero wait states during real-time execution. This lets you display and modify emulation memory without interrupting target processor execution. This capability creates a powerful nonintrusive development environment.

Extensive breakpoint capabilities are included, allowing you to define where to stop code execution. You can define unlimited software breakpoints, allowing you to halt execution at any instruction point.

Real-time hardware breakpoints increase the flexibility and power of this feature, extending functionality to include stopping at processor based on address, data and status information.

Flexible Memory Configuration

Emulation memory is available as replacement memory in your embedded design in 256K, 1M or 4M sizes mappable in 1K blocks.

Symbolic Support

Symbolic debugging clarifies trace list interpretation by allowing you to see program symbols in the trace list. This feature facilitates quick identification of problems involving the interaction between software and hardware. You can also use symbols in emulation commands and expressions to simplify command entries and user interaction.

C Debugger for PCs and Workstations

The C debugger user interface is a mouse-driven, graphical user interface for HP 64700 emulators. It runs on PCs with a Microsoft Windows 95 based interface and on an HP 9000 Series 700 workstation as an X/Motif interface. The interface offers the same look and feel on both PCs and workstations*.

The debugger gives you the ability to perform trace analysis, control program execution, set breakpoints, display variables and establish emulator configuration parameters. It takes full advantage of the emulator's dual-bus architecture and dual-ported memory to perform many C and assembly debug functions while the target runs at full speed. This means that you can handle C debugger functions such as setting breakpoints, displaying and editing C variables and measuring C program execution. Traditionally such functions could only be performed when the user program was stopped.

The debugger supports language tools from Hitachi, which provides software tools compatible with the HP E3471A emulators*. The Hitachi toolset includes a C cross-compiler and assembler which runs on PCs and HP 9000 Series 700 workstations**.

Terminal-Mode Operation

A firmware-resident ASCII terminal interface is embedded in the emulator, supplying commands for all emulation and analysis features. Commands are ASCII strings; the system accepts file transfers using industry-standard formats. Because any terminal can access these commands host independence is possible.

* For support on Sun SPARC workstations contact you local HP sales representative

** For support of IAR SYSTEMS AB assembler and compiler contact your local HP sales representative.

HP E3471A Specifications

Processor Compatibility	
Model E3471A:	Hitachi H8S/2241,2242, 2245, 2246. 2653, 2255,
Electrical	
Maximum Clock Speed:	E3471A (5 V) :25 MHz E3471A (3 V) :13 MHz with no-wait states required for emulation or target system memory.
Minimum Clock Speed:	E3471A : 32 KHz
Operation Voltage:	2.7 — 5.25 V
Power:	Primary power supplied by HP 64700 card cage
Environmental	
Temperature:	Operating, 0 to +40 °C (+32 to +104 F); Non-operating, —40 to +60 °C (—40 to 140 F)
Altitude:	Operating, 4600 m (15,000 ft); Non-operating, 15300 m (50,000 ft)
Regulatory Compliance when installed in HP 64700 card cage	
Electromagnetic Interference:	EN55011 (CISPR Group1 Class A)
Safety:	E3471A is self-certified to IEC 1010-1 and CSA-C22.2
Physical	
Cable length:	Probe to card cage approximately 0.6 m (24“)
Dimensions:	see figures 2 - 5.

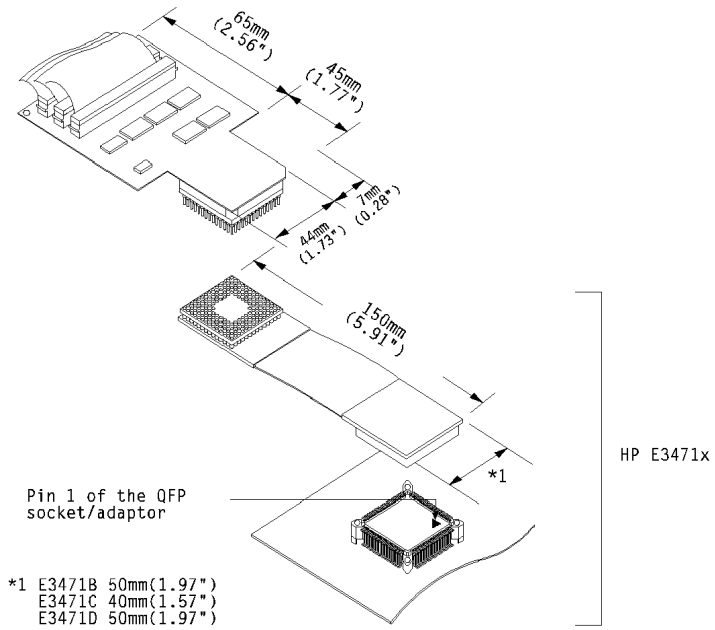


Figure 2. Adapters and Cable Dimensions

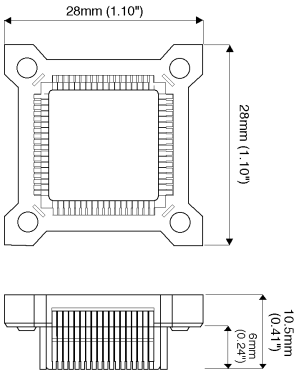


Figure 3. 120 pin QFP Socket Adapter Dimensions for HP E3471B (HP P/N E3471-61620)

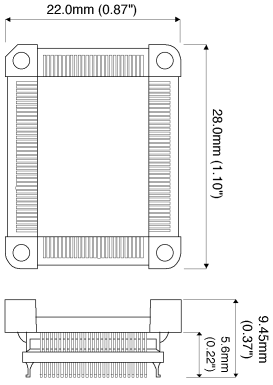


Figure 4. 128 pin QFP Socket Adapter Dimensions for HP E3471C (HP P/N E3471-61621)

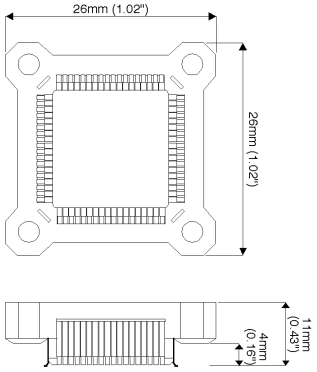


Figure 5. 100 pin QFP Socket Adapter Dimensions for HP E3471D (HP P/N E3471-61622)

Notice for the QFP Socket Adapter

The QFP Socket Adapter is an expendable supply because the electrical contacts degrade gradually as the flexible probe cables attached and detached.

One QFP socket adapter is supplied with each of HPE3471B, C, and D. Please prepare some spares of the QFP socket adapter in advance.

HP E3471A AC Timing Specifications
Vcc = 5 V, f = 20 MHz

Characteristics	Symbol	H8S/2655		HP E3471A		Unit
		min.	max.	Typical*1	Worst	
Clock cycle time	tCYC	50	500	-	-	ns
Clock pulse high width	tCH	20	-	24	10	ns
Clock pulse low width	tCL	20	-	21	10	ns
Clock rise time	tCr	-	5	2	15	ns
Clock fall time	tCf	-	5	3	15	ns
Crystal oscillator setting time(reset)	tOSC1	10	-	10	10	ms
Crystal oscillator setting time (software standby)	tOSC2	10	-	10	10	ms
External clock output setting delay time	tDEXT	500	-	500	500	us
/RES setup time	tRESS	200	-	-	275	ns
/RES pulse width	tRESW	20	-	-	20	tcyc
NMI reset setup time	tNMIRS	200	-	-	260	ns
NMI reset hold time	tNMIRH	200	-	-	200	ns
NMI setup time	tNMIS	150	-	-	225	ns
NMI hold time	tNMIH	10	-	-	10	ns
Interrupt pulse width	tNMIW	200	-	-	235	ns
IRQ setup time	tIRQS	150	-	-	180	ns
IRQ hold time	tIRQH	10	-	-	10	ns
IRQ pulse width	tIRQW	200	-	-	200	ns
Address delay time	tAD	-	20	12	35	ns
Address setup time	tAS	10	-	18	-5	ns
Address hold time	tAH	15	-	22	0	ns
Pre-charge time	tPCH	55	-	75	45	ns
CS delay time 1	tCSD1	-	20	11	35	ns
CS delay time 2	tCSD2	-	20	12	35	ns
CS pulse width	tCSW	105	-	119	95	ns
Address strobe delay time	tASD	-	30	12	45	ns
Read strobe delay time 1	tRSD1	-	30	10	45	ns
Read strobe delay time 2	tRSD2	-	30	9	45	ns
CAS delay time	tCASD	-	20	11	35	ns
Read data setup time	tRDS	15	-	15	45	ns
Read data hold time	tRDH	0	-	0	0	ns
Read data access time 1	tACC1	-	25	25	-5	ns
Read data access time 2	tACC2	-	75	75	45	ns
Read data access time 3	tACC3	-	125	125	95	ns
Read data access time 4	tACC4	-	175	175	145	ns
Read data access time 5	tACC5	-	225	225	195	ns
WR delay time 1	tWRD1	-	30	12	45	ns
WR delay time 2	tWRD2	-	30	9	45	ns
Write data strobe pulse width 1	tWSW1	30	-	42	20	ns
Write data strobe pulse width 2	tWSW2	55	-	68	45	ns
Write data delay time	tWDD	-	30	21	45	ns
Write data setup time	tWDS	0	-	12	-15	ns
Write data hold time	tWDH	10	-	10	-5	ns
WR setup time	tWCS	15	-	18	0	ns
WR hold time	tWCH	15	-	17	0	ns
/CAS setup time	tCSR	15	-	20	0	ns
WAIT setup time	tWTS	30	-	30	60	ns
WAIT set hold time	tWTH	5	-	5	5	ns
BREQ setup time	tBRQS	30	-	30	60	ns
BACK delay time	tBACD	-	30	11	45	ns
Bus floating time	tBZD	-	50	50	65	ns
BREQO delay time	tBRQOD	-	30	15	45	ns
/DREQ setup time	tDRQS	30	-	-	60	ns
/DREQ hold time	tDRQH	10	-	-	10	ns
/TEND delay time	tTED	-	30	-	45	ns
DACK delay time 1	tDACD1	-	30	-	45	ns
DACK delay time 2	tDACD2	-	30	-	45	ns

* 1 Typical outputs measured with 50pF load

HP E3471A AC Timing Specifications
Vcc = 3 V, f = 10 MHz

Characteristics	Symbol	H8S/2655		HP E3471A		Unit
		min.	max.	Typical*1	Worst	
Clock cycle time	tCYC	100	500	-	-	ns
Clock pulse high width	tCH	35	-	46	35	ns
Clock pulse low width	tCL	35	-	47	35	ns
Clock rise time	tCr	-	15	4	15	ns
Clock fall time	tCf	-	15	3	15	ns
Crystal oscillator setting time(reset)	tOSC1	20	-	20	20	ms
Crystal oscillator setting time (software standby)	tOSC2	20	-	20	20	ms
External clock output setting delay time	tDEXT	500	-	500	500	us
/RES setup time	tRESS	200	-	-	275	ns
/RES pulse width	tRESW	20	-	-	20	tcyc
NMI reset setup time	tNMIRS	200	-	-	260	ns
NMI reset hold time	tNMIRH	200	-	-	200	ns
NMI setup time	tNMIS	150	-	-	225	ns
NMI hold time	tNMIH	10	-	-	10	ns
Interrupt pulse width	tNMIW	200	-	-	235	ns
IRQ setup time	tIRQS	150	-	-	180	ns
IRQ hold time	tIRQH	10	-	-	10	ns
IRQ pulse width	tIRQW	200	-	-	200	ns
Address delay time	tAD	-	40	12	40	ns
Address setup time	tAS	20	-	43	20	ns
Address hold time	tAH	30	-	46	25	ns
Pre-charge time	tPCH	110	-	147	110	ns
CS delay time 1	tCSD1	-	40	12	40	ns
CS delay time 2	tCSD2	-	40	11	40	ns
CS pulse width	tCSW	210	-	247	210	ns
Address strobe delay time	tASD	-	60	10	60	ns
Read strobe delay time 1	tRSD1	-	60	9	60	ns
Read strobe delay time 2	tRSD2	-	60	10	60	ns
CAS delay time	tCASD	-	40	11	40	ns
Read data setup time	tRDS	30	-	30	45	ns
Read data hold time	tRDH	0	-	0	0	ns
Read data access time 1	tACC1	-	50	50	45	ns
Read data access time 2	tACC2	-	100	100	95	ns
Read data access time 3	tACC3	-	150	150	145	ns
Read data access time 4	tACC4	-	200	200	195	ns
Read data access time 5	tACC5	-	250	250	245	ns
WR delay time 1	tWRD1	-	60	11	60	ns
WR delay time 2	tWRD2	-	60	11	60	ns
Write data strobe pulse width 1	tWSW1	60	-	94	60	ns
Write data strobe pulse width 2	tWSW2	100	-	144	100	ns
Write data delay time	tWDD	-	60	18	60	ns
Write data setup time	tWDS	0	-	37	0	ns
Write data hold time	tWDH	20	-	20	20	ns
WR setup time	tWCS	30	-	44	25	ns
WR hold time	tWCH	30	-	43	25	ns
/CAS setup time	tCSR	30	-	44	25	ns
WAIT setup time	tWTS	60	-	60	60	ns
WAIT set hold time	tWTH	10	-	10	10	ns
BREQ setup time	tBRQS	60	-	60	60	ns
BACK delay time	tBACD	-	60	9	60	ns
Bus floating time	tBZD	-	100	100	100	ns
BREQO delay time	tBRQOD	-	60	13	60	ns
/DREQ setup time	tDRQS	40	-	-	60	ns
/DREQ hold time	tDRQH	10	-	-	10	ns
/TEND delay time	tTED	-	60	-	60	ns
DACK delay time 1	tDACD1	-	60	-	60	ns
DACK delay time 2	tDACD2	-	60	-	60	ns

* 1 Typical outputs measured with 50 pF load

Ordering Information

HEWLETT® PACKARD

Terminal-Based Emulation System

Model	Description
E3471A	25-MHz emulator card for H8S/2241/42/45/46 and 2653/55
E3471x*	Flexible probe cables
64794A	8 K-deep emulation bus analyzer card, 80 channels
64172B	1 MB SRAM memory module (20 ns)
64700B	Card cage

* See Flexible Cable Configuration

Emulation System Options

E3471B	120-pin flexible cable
E3471C	128-pin flexible cable
E3471D	100-pin flexible cable
64172A	256-KB, SRAM memory module (20 ns)
64173A	4 MB, SRAM memory module (25 ns)
64704A	1 K-deep 80-channel emulation bus analyzer card
64794C	64 K-deep emulation bus analyzer card, 80 channels
64794D	256 K-deep emulation bus analyzer card, 80 channels

Software Options for Workstations

For each software model number ordered, purchase one media option and at least one license option for each concurrent user.

Media/License Options

B3752A	C debugger user interface
Opt AAY*	HP 9000 Series 700 manuals/media (DDS DAT tape)
Opt UBY	HP 9000 Series 700 single-user license
Opt AJ4**	IBM-PC manual/media (3.5” floppy disc)
Opt UDY	IBM-PC single-user license

* HP Unix 9.0 or later

** Windows 95 only and only with 64700B

Flexible Cable Configuration

Processor	Pin Count	Package Type QFP	Package Type TQFP	Configuration of Emul.bd. + Flex. Cable
H8S/2653/55	120	none	Yes (.4)	E3471A + E3471B
H8S/2653/55	128	Yes (.5)	none	E3471A + E3471C
H8S/2241/42/45/46	100	Yes (.5)	Yes (.5)	E3471A + E3471D

Yes —Package is supported
No —Package is not supported
( ) —Pin pitch (mm)

Software Support

HP provides support (support via telephone and software upgrades) through the purchase of the service contract. Contact your HP field engineer for more information.

For more information on Hewlett-Packard Test & Measurement products, applications or services please call your local Hewlett-Packard sales offices. A current listing is available via Web through Access HP at http://www.hp.com. If you do not have access to the internet please contact one of the HP centers listed below and they will direct you to your nearest HP representative.

United States:
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Santa Clara, CA 95052-8059
1 800 452 4844

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Data subject to change.
Printed in U.S.A. 08/96
5965-3342E